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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,412	12/21/2001	Mark Carson	673-1030	5703

7590 04/06/2005

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EXAMINER	
PEARSON, YVETTE B	

ART UNIT	PAPER NUMBER
2144	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,412	CARSON ET AL.	
	Examiner	Art Unit	
	Yvette Pearson	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *December 21, 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 22 are presented for examination in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that f form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 16, 18, 19, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Enomoto et al. (US 5,923,384).

3. As per Claims 1 and 21, Enomoto teaches a digital data transmission apparatus (Column 2, Lines 19 – 24; Figure 6) comprising a payload data arranged in accordance with a frame structure (Figures 1B, 2B), the apparatus comprising a first switching component ([Input Side Routing Apparatus] Figure 6 #20A) for a high order data structure ([first data transmission packet] Column 4, Lines 6 – 14); a second switching component ([Signal Processing Devices] Column 4, Lines 14 – 21; Column 11, Lines 27 – 36; Figure 6, #30) being subtended from first switching component (Column 3, Lines 11 – 14); an adaptation apparatus for receiving normal (standard) data frames to a reference timing signal (transmission speed) wherein the apparatus is arranged to advance the payload data of a data frame ([input and output routing carried out by

regarding these data as the same] Column 10, Lines 40 – 48); and receiving data frame for which the payload data has been advanced to generate an output data frame comprising payload data arranged in standard frame structure with respect to receiving data frame ([SDI/SDDI data conversion to a resulting output structure] Column 14, Lines 39 - 54; Figure 6, #60.)

4. As per Claim 2, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 1 wherein data frames received by the switching apparatus is arranged to advance the payload data (data portion) of a data frame with respect to the fixed overhead of the data frame (Column 4, Lines 37 – 41.)

5. As per Claims 3 - 6 Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 1 wherein data frames further comprise one or more high order pointers and the payload data comprises one or more low order data structures, which indicate the position or value of the low order data structure, such that the adaptation apparatus is arranged to advance the payload data by advancing the position of the low order pointer ([the hierarchical structure of the digital data transmission apparatus] Column 16, Lines 41 – 58; Figure 11.)

6. As per Claim 7, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 1 wherein the payload data is advanced by an amount corresponding to the delay incurred by a data frame in passing through the first switching component and the second switching component ([input and output data transmission carried out by regarding these data as the same] Column 10, Lines 40 – 48.)

7. As per Claims 8 and 9, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 1 wherein the second switching component (SDDI data conversion device, Figure 7, #312) includes a plurality of data Memories (Figure 9, #336, #340), whereby the second switching component reads and writes successive blocks of received data to Memories ([the Video and Audio Signal Decoders read respective data, and write decoded data to Memory] Figure 9, #334, #338); and in order to align data in sequence from memories, the data are controlled by reference signals ([Frame Synchronization Signal] Figure 9, #344) to output sequenced signals (Column 14, Lines 12 – 24.)

8. As per Claim 10, Enomoto teaches a digital data transmission apparatus as disclosed above wherein the second switching component (SDDI data conversion device, Figure 7, #312) comprises a write pointer generator for controlling the writing of data blocks to the Memory ([the Video and Audio Signal Decoders write decoded data to memory] Figure 9, #334, #338) and a read pointer generator for controlling the reading of data blocks from the Memory ([the Composing Circuit composes the decoded video signal and audio from the Memory (Figure 9, #342, #344), such that the operation of the write generator is controlled by a first timing reference signal (SDDI transmission signal) and the operation of read pointer generator is controlled by a second timing reference signal (SDI transmission signal) wherein the timing reference signals are independent ([the SDDI conversion device performs signal conversion from the SDDI format to the SDI format whereby the Memories are buffers for matching the timings of the two {independent} decoded signals.] Column 14, Lines 8 – 11; Figure 9.)

9. As per Claims 11 and 12, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 10 wherein the second switching component connects with a signal reference apparatus (the Control Device, Figure 7, #20A, #40A) to be arranged to receive the system timing reference signal (Figure 7, #60) to route the first and second transmission reference signals ([Control Devices rout control information to Conversion Devices, Column 11, Lines 43 - 53) wherein the first and second timing reference signals are synchronized to the system reference timing signal ([the signal processing system performs signal routing of the SDI and SDDI format] Column 2, Lines 19 – 24.)

10. As per Claims 13 and 14, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 10 wherein the first timing reference signal is arranged to cause the writing of the data to memory at the same time as the first block of payload data is received by the switching component or to suspend writing of data to memory while fixed overhead data is received ([routing operation is set by the operator via control terminal of the output side routing apparatus] Column 11, Lines 43 – 53; Figure 7, #70A.)

11. As per Claim 15, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 10 wherein the overhead generator (the Control Device, Figure 6, #20A, #40A) is responsive to the second reference signal to generate overhead data ([the Input Side Routing Control Device controls the routing transmission between the first and second input devices] Column 11, Lines 43 – 53; Figure 7, #70A), such that the pointer generator (Conversion Device, Figure 7, #312) is arranged to

generate data in order to create an output data frame ([the Composing Circuit of the Conversion Device composes the decoded video and audio signal from the Memory and the Frame Synchronization Circuit synchronizes the composed signal with the signal of the SDI format in units of frames] Column 14, Lines 12 – 24; Figure 9, # 336, #342, #344.)

12. As per Claim 16, Enomoto teaches a digital data transmission apparatus as disclosed above in Claim 10 wherein the overhead generator (the Control Device, Figure 6, #20A, #40A) is arranged to generate fixed data denoting the beginning of an output data frame (EAV code portion) whereby the pointer generator (Composing Circuit, Figure 9, #342, #344) being arranged to cause a first payload data block to be read from Memory after data is generated (Column 2, Lines 42 – 56.)

13. As per Claim 18, Enomoto teaches a digital data transmission system comprising a synchronous transmission apparatus wherein the switching apparatus (routing apparatus) can be carried out by regarding the SDI and SDDI format as the same (Column 10, Lines 40 - 48.)

14. As per Claim 19, Enomoto teaches a digital data transmission system comprising a synchronous transmission system wherein the switching apparatus (routing apparatus) includes a data transmission system for providing a first transmission packet of the SDI format for supplying data to a second data packet of the SDDI format (Column 2, Lines 42 - 56.)

15. As per Claim 22, Enomoto teaches a digital data transmission apparatus wherein low order data structures are received as an input data frame ([Input Device data of the

SDI/SDDI format provide input to the Input Side Routing Apparatus] Column 11, Lines 23 – 26; Figure 6, #10; Figure 1A; Figure 2A), generating an output data frame comprising payload data wherein the apparatus further includes a plurality of data memories and is arranged to write successive blocks of received payload data in sequence to create an output data frame (Column 11, Lines 27 – 36); such that the writing and reading of data from Memory is controlled by respective independent time reference signals; the second switching component (SDDI data conversion device, Figure 7, #312) comprises a write pointer generator for controlling the writing of data blocks to the memory ([the Video and Audio Signal Decoders write decoded data to memory] Figure 9, #334, #338) and a read pointer generator for controlling the reading of data blocks from the memory ([the Composing Circuit composes the decoded video signal and audio from the memory (Figure 9, #342, #344), such that the operation of the write generator is controlled by a first timing reference signal (SDDI transmission signal) and the operation of read pointer generator is controlled by a second timing reference signal (SDI transmission signal) wherein the timing reference signals are independent ([the SDDI conversion device performs signal conversion from the SDDI format to the SDI format whereby the Memories are buffers for matching the timings of the two {independent} decoded signals.] Column 14, Lines 8 – 11; Figure 9.)

16. Thus, Enomoto discloses all limitations of the rejected claims; therefore Enomoto anticipates the subject matter of Claims 1 – 16, 18, 19, 21 and 22.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enomoto et al. (US 5,923,384) in view of Klish et al (US 6,014,708).

18. With respect to Claims 17 and 20, Enomoto teaches a digital data transmission apparatus comprising a first switching component ([Input Side Routing Apparatus] Figure 6 #20A) for a high order data structure ([first data transmission packet] Column 4, Lines 6 – 14); a second switching component ([Signal Processing Devices] Column 4, Lines 14 – 21; Column 11, Lines 27 – 36; Figure 6, #30) being subtended from first switching component (Column 3, Lines 11 – 14); and receiving data frame for which the payload data has been advanced to generate an output data frame comprising payload data arranged in standard frame structure with respect to receiving data frame (Column 14, Lines 39 - 54; Figure 6, #60), but fails to specifically teach a network arranged to switch data frames that are compliant with Synchronous Digital Hierarchy (SDH) and/or Synchronous Optical Network (SONET) Standards. However Klish teaches a method for mapping an Ethernet payload to a synchronous payload of a SONET /SDH output

signal providing a fast payload input signal wherein the amount of data transmitted is increased per unit time of the standard Ethernet output line (Column 2, Lines 18 – 29.)

Therefore, it would have been obvious to one having ordinary skill in the art having the teachings of Enomoto and Klish before one at the time of the invention to include Synchronous Digital Hierarchy (SDH) and/or Synchronous Optical Network (SONET) Standards, because Enomoto provides a digital data transmission apparatus which can suitably route a signal of the SDI format and a signal of the SDDI format and further has a conversion device which can perform conversion between the signal of the SDI format and the signal of the SDDI format with a high efficiency (Column 2, Lines 31 – 36) such that digital data transmission can be improved by adopting various structures (Column 17, Lines 23 – 31, Lines 38 – 40.) The combination would have provided a data conversion system having a transmission signaling capacity fully utilized to improve the effectiveness for routing digital data of different types.

Conclusion

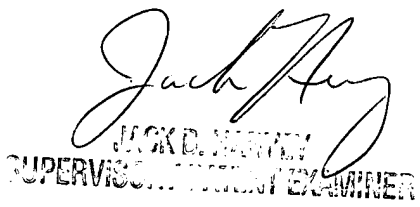
19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

20. US 5,282,206, (Ishihara et al.) discloses a synchronous circuit that establishes frame synchronism by using pointers in a digital transmission system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yvette Pearson whose telephone number is 571 272-4227. The examiner can normally be reached on 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Cuchlinski can be reached on 571 272-3925. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Yvette Pearson

Examiner

Art Unit 2144